In the claims:

Please cancel claims 1-22.

Please add new claims 23-28 as follows:

1- 22 (Cancelled)

23. (new) In a digital system of the type having at least first and second processors and at least one shared resource accessible to the processors via a system bus, the bus allowing only one bus transaction in any one clock cycle, a hardware semaphore circuit coupled to said system bus and configured to monitor shared resource accesses by said processors, the hardware semaphore circuit comprising:

a semaphore cell coupled to the first and second processors via the system bus and configured to have a first state and a second state, the first state indicating that the shared resource is available for access and the second state indicating that the shared source is unavailable for access, and configured to be in the second state after being read by any processor and to change back to the first state after the shared resource is again made available for access; and

an interrupt generation circuit coupled to the first and second processors via the system bus and coupled to an output of the semaphore cell, and configured to generate a semaphore interrupt signal to any processor requesting access to the shared resource whenever the semaphore cell changes from the second state back to the first state, the interrupt generation circuit comprising:

(i) a semaphore interrupt cell coupled to the output of the semaphore cell and configured to have a third state and a fourth state, the fourth state indicating that the semaphore cell has changed from the second state back to the

first state and thus that the shared resource has just been made available for access;

(ii) first and second semaphore interrupt enable cells respectively coupled to the first and second processors via the system bus, each semaphore interrupt enable cell configured to have a fifth state and a sixth state, the fifth state indicating that the corresponding processor does not need to access the shared resource and the sixth state indicating that the corresponding processor has read the semaphore cell and found that the semaphore is in the second state; and

(iii) first and second logic gate circuits coupled to the semaphore interrupt cell, to respective first and second semaphore interrupt enable cells, and via the system bus to respective first and second processors, each logic gate circuit configured to generate a semaphore interrupt signal to its corresponding processor if the semaphore interrupt cell is in the fourth state and the corresponding semaphore interrupt enable cell is in the sixth state, the semaphore interrupt cell and a corresponding semaphore interrupt enable cell further configured to change back to their respective third and fifth states after the semaphore interrupt signal is sent to its corresponding processor.

24. (new) The hardware semaphore circuit in a digital system as in claim 23, wherein the system has multiple shared resources, and the semaphore cell, the semaphore interrupt cell and the first and second semaphore interrupt enable cells are cells of corresponding registers with one cell of each register dedicated to semaphore operations for a particular shared resource.

25. (new) The hardware semaphore circuit in a digital system as in claim 23, wherein more than two processors can access the at least one shared resource via the system bus, and the interrupt generation circuit comprises additional semaphore interrupt enable cells and logic gate circuits corresponding each additional processor.

26. (new) The hardware semaphore circuit in a digital system as in claim 23, wherein the semaphore cell comprises (i) a semaphore address input bus, a read/write control input line, and a semaphore data output line, all coupled to the system bus, (ii) an address decoder coupled to the semaphore address input bus and configured to generate a signal in response to a unique address associated with the semaphore cell for the shared resource, (iii) a multiplexer having a first input, a second input coupled to the read/write control input line, a control input coupled to receive the signal generated by the address decoder, and an output, the multiplexer configured to connect its second input to its output in response to receiving the signal from the address decoder but otherwise to connect its first input to its output, (iv) a flip-flop having a data input coupled to the output of the multiplexer and a data output coupled to the semaphore interrupt cell as an output of the semaphore cell and to the first input of the multiplexer, (v) an AND gate having a first input coupled to receive the signal generated by the address decoder, a second input coupled to the read/write control input line, and an output, and (vi) a buffer having a buffer input coupled to the output of the flip-flop, an enable input coupled to the output of the AND gate, and a buffer output coupled via the semaphore data output line to the system bus.

27. (new) The hardware semaphore circuit in a digital system as in claim 23, wherein the semaphore interrupt cell comprises (i) a first flip-flop having a data input coupled to the output of the semaphore cell, and a data output, (ii) an AND gate having a first input coupled to the output of the semaphore cell and a second input coupled to the output of the first flip-flop, one of the data input of the first flip-flop and the first input of the AND gate being an inverted input, the AND gate also having an output, (iii) an OR gate having a first input, a second input coupled to the output of the AND gate, and an output, and (iv) a second flip-flop having a data input coupled to the output of the OR gate and a data output coupled to the first input of the OR gate, the data output of the second flip-flop forming the output of the semaphore interrupt cell.

28. (new) A method of using a hardware semaphore circuit to monitor shared resource accesses over a system bus that allows only one bus transaction in any one clock cycle, there being at least first and second processors and at least one shared resource coupled to said system bus together with said hardware semaphore circuit, the method comprising:

reading a state of a semaphore cell of the hardware semaphore circuit by a first processor and if the state read from the semaphore cell is a first state, indicating that the shared resource is available for access, then accessing the shared resource by the first processor, but if the state read from the semaphore cell is a second state, indicating that the shared resource is unavailable for access, then setting a first semaphore interrupt enable cell to a state indicating that the first processor needs to access the shared resource and the first processor waiting for a semaphore interrupt signal from the hardware semaphore circuit before again reading the state of the semaphore cell, any reading of the

state of the semaphore cell by any processor setting the state of the semaphore cell to its second state, the semaphore cell changing back to its first state after the shared resource is again made available for access;

continually monitoring the state of the semaphore cell by a semaphore interrupt cell of the hardware semaphore, the semaphore interrupt cell having third and fourth states with the fourth state indicating that the shared resource has just been made available for access, the semaphore interrupt cell changing to the fourth state whenever the semaphore cell being monitored has just changed from the second state back to the first state;

reading the state of the semaphore cell by a second processor and if the state read from the semaphore cell is a first state then accessing the shared resource by the second processor, but if the state read from the semaphore cell is second state then setting a second semaphore interrupt enable cell to a state indicating that the second processor reads to access the share resource and the second processor waiting for a semaphore interrupt signal from the hardware semaphore circuit before again reading the state of the semaphore cell; and

whenever the semaphore interrupt cell changes to the fourth state and either the first or second semaphore interrupt enable cell is in a state indicating that the respective first or second processor needs to access the shared resource, generating a semaphore interrupt signal for the respective first and second processor and transmitting said interrupt signal thereto over said system bus.